IN THE CLAIMS:

Please cancel claims 1-4 and 11-13 and 15 without prejudice or disclaimer, amend claims 5-6, 8-10 and 14, and add new claims 18-19 as follows:

1-4. (Cancelled)

5. (Currently Amended) The signal communication apparatus according to claim 14 [[1]], further comprising an input terminal for a selection signal for changing the selection of the single clock signal ~~a bits~~ in the clock signal ~~extraction~~/selection circuit.

6. (Currently Amended) The signal communication apparatus according to claim 14 [[1]], further comprising a clock signal monitoring circuit that monitors the voltage level or frequency of the selected reference clock signal or the clock signals extracted from the ~~reference clock signal or~~ data signals and which, if it detects abnormality in the voltage level or frequency, outputs a control signal for switching the reference clock signal to a normal clock signal extracted from a different data signal bit.

7. (Original) The signal communication apparatus according to claim 6, further comprising an alarm means for indicating the occurrence of an abnormality in the event of detection of an abnormality by the clock signal monitoring circuit.

8. (Currently Amended) The signal communication apparatus according to claim 14 [[I]], further comprising a data signal monitoring circuit that monitors at least one kind of information about the communication quality of the data signal from which the reference clock signal is to be extracted, the information being selected from the group consisting of voltage level, rise and fall edges, presence or absence of bit error, bit error ratio, and the amount of jitter.

9. (Currently Amended) The signal communication apparatus according to claim 8, further comprising an alarm means for notifying ~~indicating~~ the occurrence of an abnormality in the event that the data signal monitoring circuit detects an abnormality.

10. (Currently Amended) The signal communication apparatus according to claim 14 [[1]], further comprising a data signal monitoring circuit that monitors at least one kind of information about the communication quality of the redigitized n-bit data signals, the information being selected from the group consisting of voltage level, presence or absence of bit error, bit error ratio, and the amount of jitter, wherein, if the information about the communication quality exceeds a predetermined tolerance value, the monitoring circuit deems the relevant bit unfit for communication and produces a data signal abnormality notifying signal.

11-13. (Cancelled)

14. (Currently Amended) A signal communication apparatus of the clock reproduction transmission type in which communication is conducted using parallel optical or electric signals, the apparatus comprising a data signal reception section for receiving data signals that have been transmitted, wherein the data signal reception section comprises:

a number a of clock signal extraction circuits, each of which extracting a clock signal from each of a-bit data signals in n-bit parallel data signals that have been received, where a is an integer such that $2 \leq a < n$;

a clock signal selection circuit for selecting a single clock signal from the extracted a clock signals, the single clock signal being designated as a reference clock signal; [[and]]

a number n of phase adjusting circuits for adjusting the phase of the selected reference clock signal to produce [[a]] reproduction clock signals for the received n-bit parallel data signals ~~each bit~~, each [[the]] reproduction clock signal providing [[the]] a timing of redigitization of each of the received n-bit parallel data signals; and

sampling means for redigitizing each of received n-bit parallel data signals in accordance with the timing provided by the reproduction clock signal for each bit.

15. (Cancelled)

16. (Original) A signal communication system of the clock reproduction transmission type in which communication is conducted using parallel optical or electric signals, the system comprising:

a data signal transmission section for transmitting parallel data signals; and

a data signal reception section for receiving the parallel data signals that have been transmitted, wherein

the data signal reception section comprises:

a clock signal extraction/selection circuit for selecting a number b of bits from a number a of bits in n-bit data signals that have been received, where a is an integer such that $2 \leq a < n$, and b is such an integer that $1 \leq b \leq a$, the clock signal extraction/selection circuit extracting a clock signal from the selected data signal and outputting it as a reference clock signal;

a number n of phase adjusting circuits for adjusting the phase of the reference clock signal to generate a reproduction clock signal for each bit, the reproduction clock signal providing the timing of redigitizing each of the n-bit data signals that have been received;

a sampling means for redigitizing each of the received n-bit data signals using the timing provided by the reproduction clock signal for each bit;

a monitoring means for monitoring each of the n-bit data signals obtained from the sampling means in terms of whether or not the data is normal; and

a data signal bit control circuit that determines the usability of the n-bit data signals in accordance with the output of the monitoring means, produces a routing control signal for routing a row of data only to normally operable data signal bits, and transmits the routing control signal to the data signal transmission section, and wherein

the data signal transmission section comprises:

an input circuit for receiving the bit routing control signal transmitted from the data signal bit control circuit in the data signal reception section; and

a routing circuit for routing a row of data to be transmitted to the normally operable data signal bits in accordance with the bit routing control signal.

17. (Original) The signal communication system according to claim 16, wherein the routing of a number c of bits of data to the remaining n-c bits that are operable (where c and n are integers such that $1 < c < n$) is conducted on a bit by bit basis, k-bit basis, or packet data basis.

18 (New) The signal communication apparatus according to claim 14, wherein the clock signal selection circuit is provided for each of a blocks of the received n-bit parallel data signals, and each output of the clock signal selection circuit for each block is distributed to phase adjusting circuits in the block as a reference clock signal for the block,

wherein said clock signal selection circuit includes circuit for switching the selection of the reference clock signal for a block, in case where a clock signal extraction circuit for the block cannot correctly extract a clock signal, to select another reference clock signal extracted in another block.

19. (New) A signal communication apparatus of the clock reproduction transmission type whereby communication is conducted using parallel optical or electrical signals, the apparatus comprising a data signal reception unit for receiving transmitted data signals, said data signal reception unit comprising:

a clock signal extraction/selection circuit for extracting clock signals from a-bit data signals in n-bit parallel data signals that have been received, where a is an integer such that $2 \leq a < n$, and outputting the extracted clock signal as a reference clock signal;

a number n of phase adjusting circuits for adjusting the phase of extract clock signals and thereby producing reproduction clock signals for the received n-bit data signals, each of the reproduction clock signals providing a timing of redigitization of each data signal; and

sampling means for redigitizing each of the received n-bit data signals in accordance with the timing provided by the reproduction clock signal for each bit,

wherein the clock signal extraction/selection circuit comprises:

a voltage controlled oscillator;

a number a of phase comparators respectively comparing the phase of each of the a-bit data signals with that of output signal of each of said voltage controlled oscillators;

a selector for selecting one output from comparison outputs of said phase comparators; and

a loop filter for connecting the selected comparison output to said voltage controlled oscillator.